

## Functional Description

The ISL6401 pulse width modulating (PWM) current mode controller is designed for a wide range of DC/DC conversion applications including boost, flyback, and isolated output configurations. The device is optimized to provide high performance, low-cost solution for Ringing SLIC (RSLIC) Ring (Vbh) and Talk (Vbl) power supplies in VoIP applications. The IC features an integrated inverter that is ideal for generating negative output voltage like RSLIC Ring Vbh (-72V) and Talk Vbl (-24V), -48V for IP Phones, -5V and -15V for DSL CO line drivers. The output voltages are adjusted with an external voltage divider.

Peak current mode control architecture effectively handles Ring trip transients and provides inherent over-current protection. Flyback topology allows the operation close to 50% duty cycle, offering optimum transformer utilization, low ripple current and less stress on input/output capacitors. Internal soft start minimizes start-up stress without any external components. The switching frequency can be programmed from 50kHz to 600kHz or alternatively the internal oscillator can be locked to an external clock fed at SYNC input for noise sensitive applications. A logic level shutdown input is included, which reduces supply current to 55µA in the shutdown mode. DC/DC conversion efficiency is optimized by use of a low current sense voltage.

For a detailed functional description, complete specifications and component selection guidelines, please refer to the *ISL6401 Data Sheet*, Intersil Corporation, File No. FN9007, available on Intersil's website, <http://www.intersil.com/>.

## Application Information

As worldwide demand for inexpensive Voice over Internet Protocol telephony grows, so will the need for Integrated Circuits that are specialized to enable compatibility between new telephony systems and older telephones based on analog standards. Analog ring signal generation and off hook loop current supply are two analog functions that are performed by Subscriber Line Interface Circuits (SLICs). This application note discusses the special power supply implementation to generate the high negative voltages needed by SLICs.

### Overview of Telephone Loop System

Traditionally a telephone network consists of a circuit between the subscriber and the central office. However, the advent of new high speed digital technologies have created the need to control and manage the functions of the phone locally as opposed to the central office. In both instances the principals governing the operation of the phone loop are essentially the same.

In a telephone loop, the subscriber is connected to the network via 2 wires, commonly known as Tip and Ring. The actual digital telecommunications trunk line however, operates on 4-wires; two of which are allocated for transmitting and two for receiving. This 2 to 4-wire interface consists of the SLIC and CODEC. A SLIC is the primary interface between the 4-wire (ground referenced) low voltage switch environment and the 2 wire (floating) high voltage loop environment. It performs a number of important functions including Battery feed, Overvoltage protection, Ringing, Signaling, Coding, Hybrid Balancing and also Testing.

The Ringing SLIC (RSLIC) typically requires two high voltage power supply inputs. The first is a tightly regulated voltage around -24V or -48V for off-hook signal transmission. The second is a loosely regulated -70 to -100V for ring tone generation. When the switch hook is released the phone puts approximately 200Ω of resistance across the phone terminals. Intersil RSLICs feature internal current limiting so this load is not presented to the power supply. However, not all of the SLICs available in the market offer this feature and the power supply is expected to maintain output during the remainder of the ring cycle. Once voice transmission begins, the SLIC, in many cases, requires a lower voltage input to establish a 20-25mA current loop. The loop feeds the 200Ω, protection resistors, and line resistances within the phone. In some cases, the lower supply and higher supply voltage are combined and the SLIC runs from a compromise voltage of approximately -53V.

The specifications below are for a 4-line requirement with 5 REN per line

**TABLE 1. TYPICAL POWER SUPPLY REQUIREMENT FOR VoIP RESIDENTIAL GATEWAY**

PARAMETER	REQUIREMENT
Input Voltage	5 or 12 volts
Output Power	3 to 10 watts
Efficiency	80 to 90%
Output Voltages	-24V, -72 to -100V and/or -48V
-24V Requirements (4 lines)	Regulation: ±5% Maximum Output Current: 0.10A Ripple: Less than 0.25Vpp
-72V Requirements (4 lines)	Regulation: ±10% Maximum Output Current: 0.10A Ripple: Less than 1Vpp

## Using the ISL6401 Evaluation Board

The ISL6401EVAL1E Schematic shows a current mode power supply using the Intersil ISL6401 in standard flyback topology. The ISL6401EVAL1 evaluation board is shipped “ready to use” right from the box. The IC requires +5V Bias. The evaluation board input voltage can be 10V to 16V with the specified transformer and external components. The output voltages are -24V at 120mA and -72V at 120mA. The board is capable of evaluating device operation with loads that simulate one, two, three or four line operation. The use of an electronic load enables evaluation over a wide range of operating conditions. Simply vary the load on each output from 0 - 120mA in any combination to match exact application requirements. The circuit uses off the shelf inexpensive transformers to generate both outputs using a single controller. The transformer turns ration is 1:1:1:1 where 24V appear across each secondary winding and the primary during the switch off time. The remaining secondary windings are stacked in series to develop -48V. The -48V section is then stacked on the -24V section to get the -72V. This technique provides good cross regulation, lowers the voltage rating required for the output capacitors and lowers the RMS current, allowing the use of cheaper output capacitors. Also, the selection of a transformer with multifilar winding lowers the leakage inductance and cost. The cross regulation of both output is achieved by using split feedback for both outputs where the feedback factor can be weighed based on load condition on both outputs.

TABLE 2. ISL6401 EVALUATION BOARD

BOARD NAME	IC	PACKAGE
ISL6401EVAL1E	ISL6401CB	14-Ld SOIC

The evaluation board kit also includes 5 samples of ISL6401CB and ISL6401CR each.

### Recommended Test Equipment

- A 5V power supply to bias the IC.
- A 12V power supply capable of supplying 2A of current
- Two electronic loads
- Precision digital multimeters
- A 4-channel scope with probes

### Power and Load Connections

The ISL6401 evaluation board has three sets of terminal posts and a jumper that are used to supply the input voltages and to monitor and load the outputs.

**Jumper Settings** - Jumper JP1 allows the ISL6401 to be biased from a separate 5V supply or from the input voltage at VIN using a zener diode.

If a 5V supply is being used for the VCC input, place a jumper connecting the pins to the left (pin 1 and pin 2) of JP1. Placing a jumper to the right (pin 2 and pin 3) of JP2 will supply the bias of the ISL6401 from the input voltage at VIN using a zener diode (D1).

**Input Voltage** - Adjust the power supplies to provide the 5V and 12V input voltages. With the power supplies turned off, connect the positive lead of the 5V supply to the VCC post (P3). Connect the ground lead of the supply to the GND post (P4). Connect the positive lead of the 12V supply to the VIN post (P1). Connect the ground lead to the GND post (P2).

**Output Voltage Loading and Monitoring** - To exercise and monitor VOUT1, connect the positive lead of one of the electronic loads to the GND post (P7). Connect the ground lead of the electronic load to the VOUT1 post (P8). Connect the positive end of a digital multimeter to the VOUT1 post (P8). Connect the digital multimeter ground terminal to the GND post (P7).

To exercise and monitor VOUT2, connect the positive lead of the other electronic load to the GND post (P10). Connect the ground lead of the electronic load to the VOUT1 post (P9). Connect the positive end of a digital multimeter to the VOUT1 post (P9). Connect the digital multimeter ground terminal to the GND post (P10).

Each output can be viewed with an oscilloscope using the two scope probes, SP1 (VOUT1) and SP2 (VOUT2).

### Startup

The ISL6401 features an internal digital soft start to reduce transformer and output capacitor stress and to reduce the inrush current surge on the input circuits. Figure 1 shows the startup sequence.

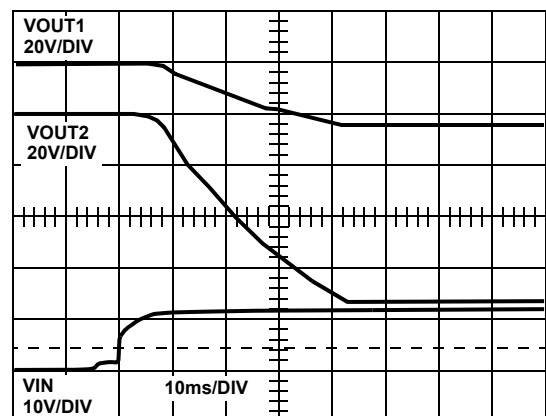


FIGURE 1. SOFT START WAVEFORMS (2ms/DIV)

**Output Performance**

**Output Ripple** - Figure 2 shows the output voltage ripple for VOUT1 and VOUT2 both at 100mA load.

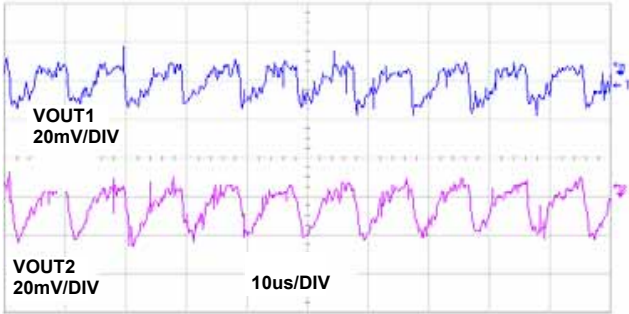


FIGURE 2. OUTPUT 1 AND 2 RIPPLE VOLTAGE

**Transient Response** - Figure 3 and Figure 4 show the transient performance of the each output for a step load from 0mA to 100mA.

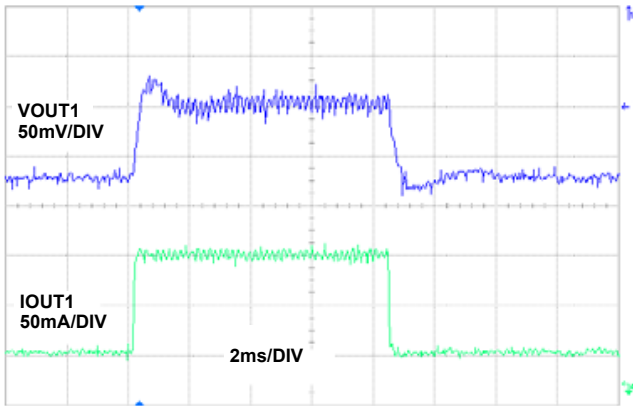


FIGURE 3. VOUT1 TRANSIENT RESPONSE

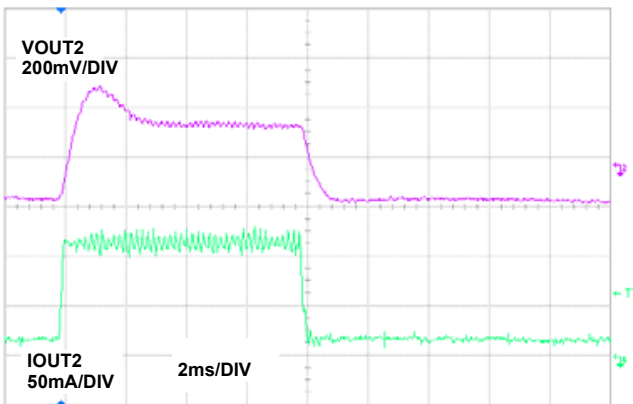


FIGURE 4. VOUT2 TRANSIENT RESPONSE

**Oscillator**

**Switching Frequency** - The gate driver output switching frequency can be programmed from 50kHz to 600kHz by adjusting the capacitor value on the CT pin (C5). Figure 5 can be used as a guideline in selecting the capacitor value required for a given frequency.

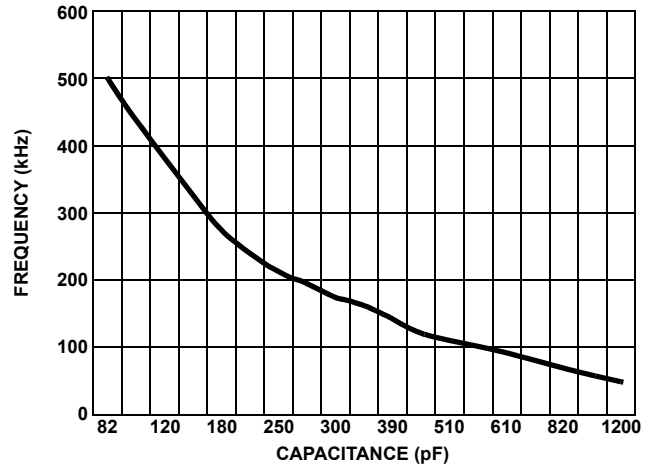


FIGURE 5. OUTPUT SWITCHING FREQUENCY vs CT

**External Synchronization** - The internal oscillator can be synchronized by an external clock connected to the SYNC pin (P6). Program the free running frequency of the oscillator to be 10% slower than the desired synchronous frequency. The external clock signal should have a minimum pulse width of 20ns.

**Shutdown**

When the SD pin (P5) is pulled low, the PWM is turned off and the output capacitors discharge. A typical shutdown waveform using the SD pin is shown in Figure 6.

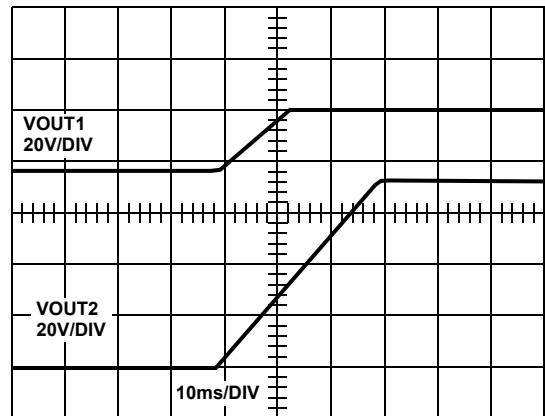


FIGURE 6. OUTPUT SHUTDOWN WAVEFORMS

**Conclusion**

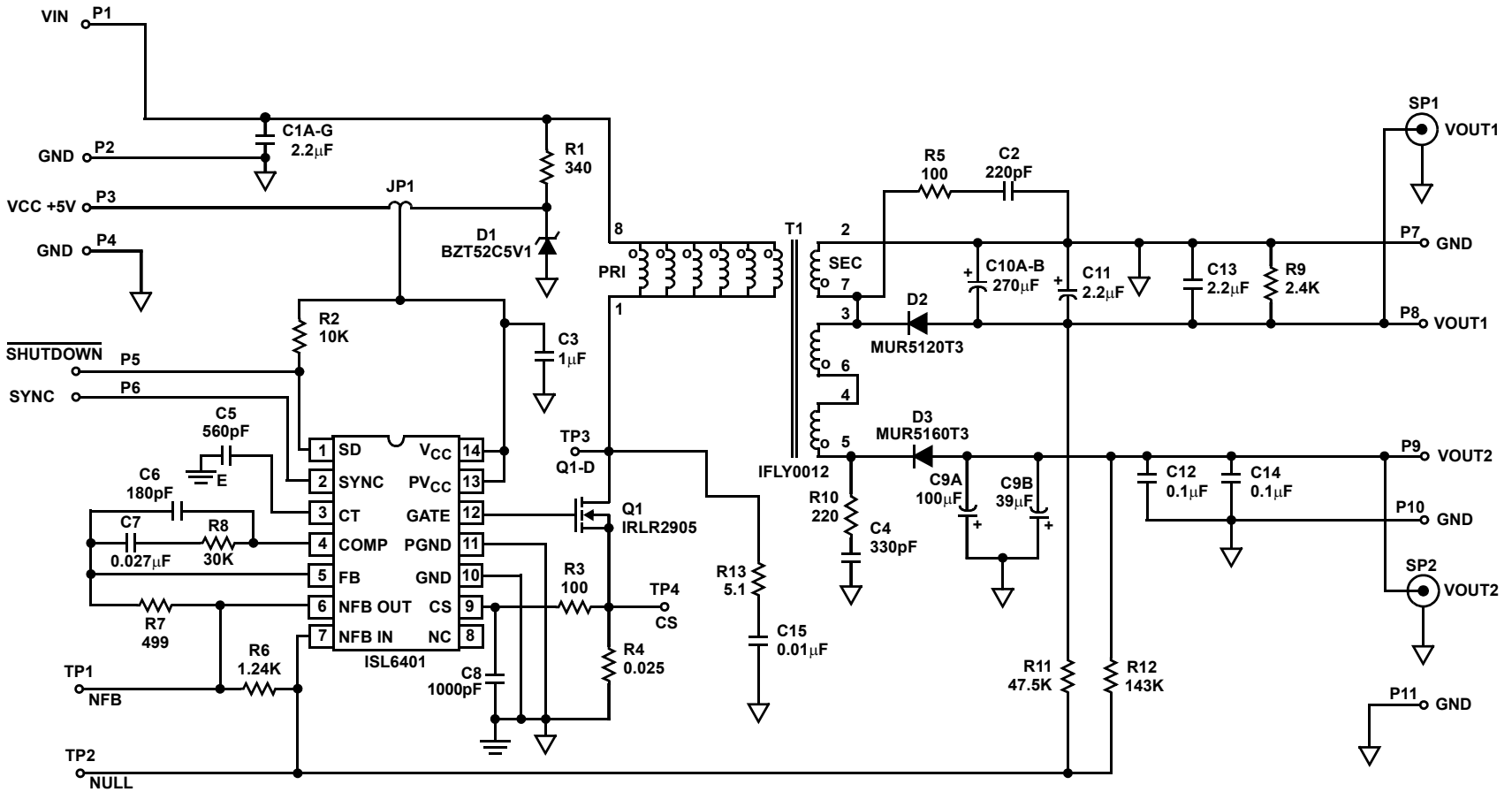
The ISL6401EVAL1 evaluation board is a flyback reference design optimized to provide a high performance, low-cost solution for RSLIC Ring and Talk power supplies in VoIP application. It has the capability of evaluating device operation with loads that simulate one, two, three, or four line operation.

**References**

1. ISL6401 Datasheet, Intersil Corporation, File No. FN9007

For Intersil documents available on the web, see <http://www.intersil.com/>

# ISL6401EVAL1E Schematic



## Application Note 1082

### ISL6401EVAL1E Bill of Materials

ITEM	REFERENCE	QTY	PART NUMBER	PART TYPE	DESCRIPTION	PACKAGE	VENDOR
1	U1	1	ISL6401CB	IC, Linear	Current mode PWM Controller	SO-14	Intersil
2	Q1	1	IRLR2905	MOSFET Single	N-channel, 55V, 0.027Ω, 42A	TO-252AA	International
3	D1	1	BZT52C5V1	Diode	Zener, 5.1V, ±5%, 0.5A	SOD123	Diode
4	D2	1	MURS120T3	Diode	Schottky, 200V, 1A	Case 403A-03	Motorola/ON Semi
5	D3	1	MURS160T3	Diode	Schottky, 600V, 1A	Case 403A-03	Motorola/ON Semi
6	T1	1	IFLY0012	Transformer	Custom Built	IFLY0012	GCI/Falco
7	C1A to C1G, C11, C13	9	GMK325BJ225KN-T	Capacitor, Ceramic	2.2μF, 20%, 35V, X7R	SM_1210	Taiyo Yuden
8	C2	1	0805YC221KAT2A	Capacitor, Ceramic, NPO	220pF, 10%, 50V	SM_0805	AVX/Panasonic
9	C3	1	1812C105MAT2A	Capacitor, Ceramic, X7R	1μF, 20%, 50V	SM_1812	AVX
10	C4	1	1206YC331KAT2A	Capacitor, Ceramic, NPO	330pF, 20%, 100V	SM_1206	AVX/Panasonic
11	C5	1	08055A561FAT2A	Capacitor, Ceramic, NPO	560pF, ±1 50V	SM_0805	AVX/Panasonic
12	C6	1	0805YC181KAT2A	Capacitor, Ceramic, NPO	180pF, 10%, 50V	SM_0805	AVX/Panasonic
13	C7	1	0805YC273KAT2A	Capacitor, Ceramic, X7R	0.027μF, 10%, 50V	SM_0805	AVX/Panasonic
14	C8	1	0805YC102KAT2A	Capacitor, Ceramic, X7R	1000pF, 5%, 50V	SM_0805	AVX/Panasonic
15	C9A	1	100MV100AX	Capacitor, Aluminum	100μF, 20%, 100V	TANT-200-500	SAYNO
16	C9B	1	100MV39AX	Capacitor, Aluminum	39μF, 20%, 100V	CASE-CC	SAYNO
17	C10A	1	35MV270AX	Capacitor, Aluminum	270μF, 20%, 35V	CASE-CC	SAYNO
18	C10B (Do Not Populate)	1		Capacitor, Aluminum		CASE-CC	SAYNO
19	C12, C14	2	1812C104MAT2A	Capacitor, Ceramic, X7R	0.1μF, 20%, 100V	SM_1812	AVX/Panasonic
20	C15	1	0805YC103KAT2A	Capacitor, Ceramic, X7R	0.01μF, 5%, 50V	SM_0805	AVX/Panasonic
21	R1	1		Resistor, Film	340Ω, 5%, 1/2W	SM_2010	Panasonic
22	R2	1		Resistor, Film	10kΩ, 1%, 0.1W	SM_0805	Panasonic
23	R3	2		Resistor, Film	100Ω, 5%, 0.1W	SM_0805	Panasonic
24	R4	1		Resistor, Power metal strip	0.025Ω, 1%, 1W	SM_2512	Vishay / IRC
25	R5	1		Resistor, Film	100Ω, 5%, 0.25W	SM_1210	Panasonic
26	R6	1		Resistor, Film	1.24kΩ, 1%, 0.1W	SM_0805	Panasonic
27	R7	1		Resistor, Film	499Ω	SM_0805	Panasonic
28	R8	1		Resistor, Film	30KΩ, 1%, 0.1W	SM_0805	Panasonic
29	R9 (Do Not Populate)	1		Resistor, Film	2.43kΩ, 1%, 1/8W	SM_01206	Panasonic
30	R10	1		Resistor, Film	220Ω, 1%, 0.25W	SM_1210	Panasonic
31	R11	1		Resistor, Film	47.5kΩ, 1%, 0.1W	SM_0805	Panasonic
32	R12	1		Resistor, Film	143kΩ, 1%, 0.1W	SM_0805	Panasonic

**ISL6401EVAL1E Bill of Materials** (Continued)

ITEM	REFERENCE	QTY	PART NUMBER	PART TYPE	DESCRIPTION	PACKAGE	VENDOR
33	R13	1		Resistor, Film	5R1Ω, 5%, 0.25W	SM_1210	Panasonic
34	JP1	1	68000-236-1X3	Jumper, 3 position	1x3 Break Strip GOLD		
35	JP1	1	S9001-ND	Jumper	2 pin jumper		Digikey
36	TP1 to TP4	4	5002	TEST POINT vertical,white	PC test jack	PTH	Keystone
37	P1 - P11	11	1514-2	Turrett Post	Terminal post,through hole,1/4 inch tall	PTH	Keystone
38	SP1, SP2	2	TEK131-4353-00	Terminal, Scope Probe	Terminal, Scope Probe		Tektronix
39	Mounting Hole 1-4	4	4-40X1/2 Screw	Screw, #4, Panhead	4-40x1/2 Screw		
40	Mounting Hole 1-4	4	4-40X3/4 Standoff- Metal	Standoff, 1", for #4 screw	4-40x3/4 Standoff-Metal	PTH = 0.250"	

**ISL6401EVAL1E Layout**

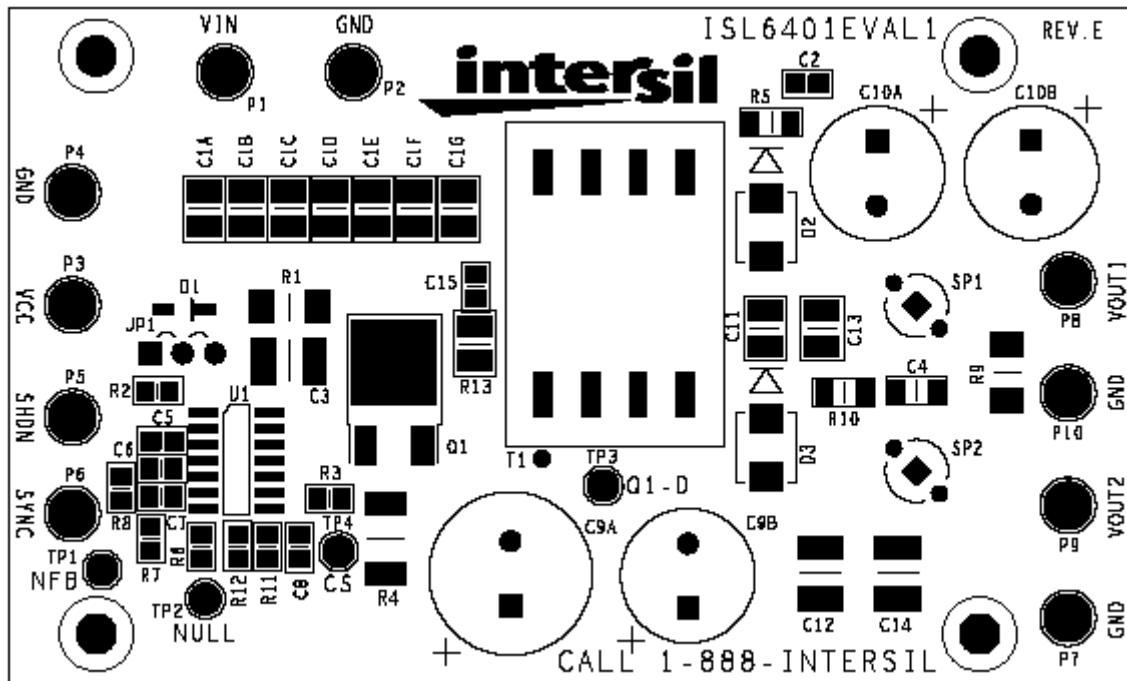


FIGURE 7. TOP SILKSCREEN

ISL6401EVAL1E Layout (Continued)

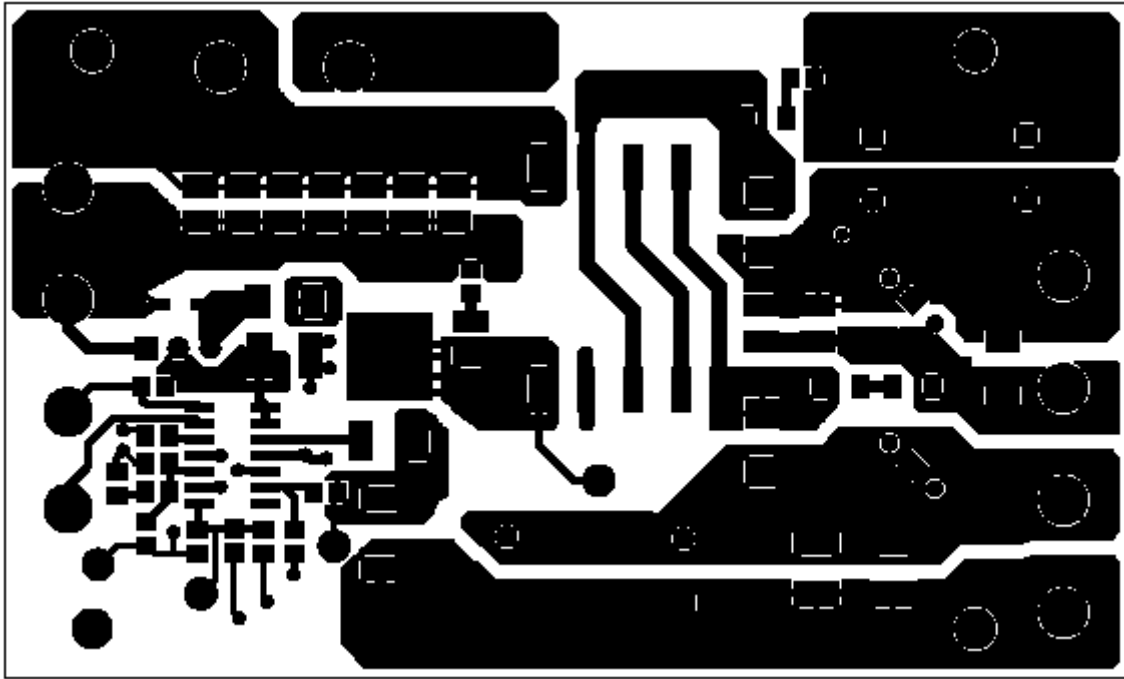


FIGURE 8. TOP LAYER 1

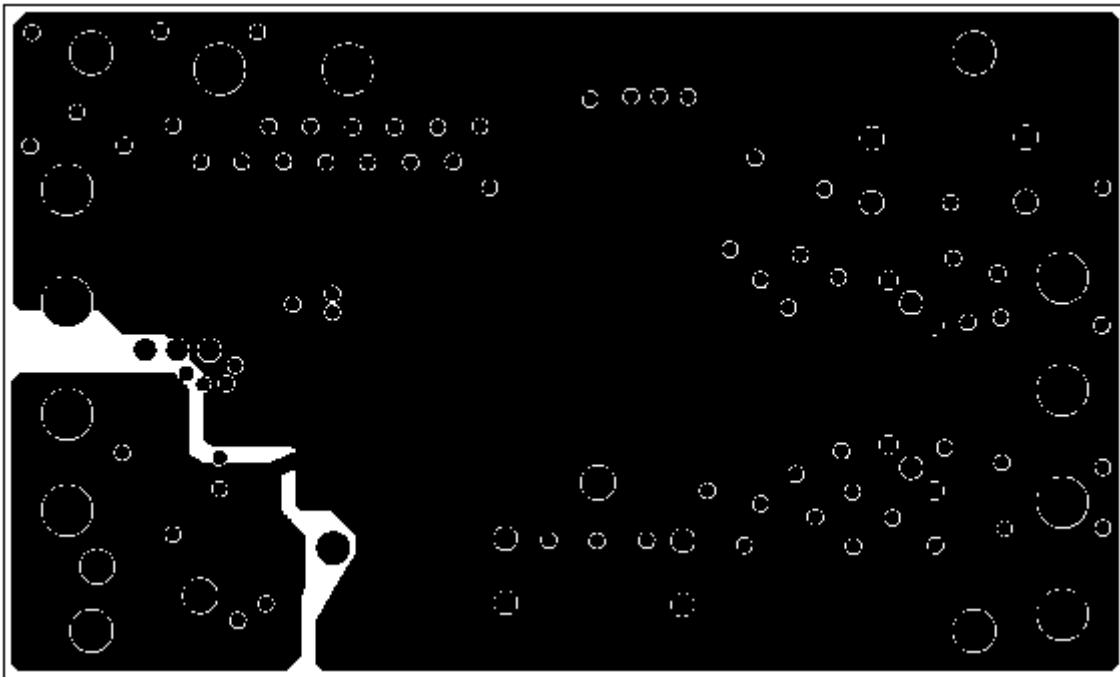


FIGURE 9. TOP LAYER 2

ISL6401EVAL1E Layout (Continued)

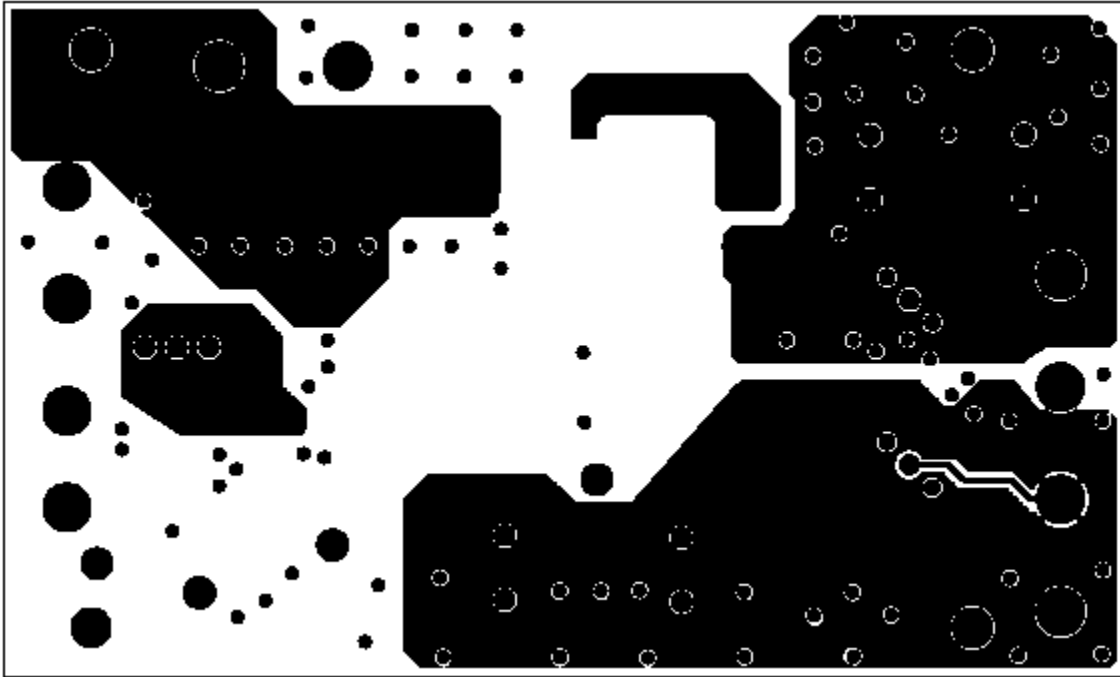


FIGURE 10. TOP LAYER 3

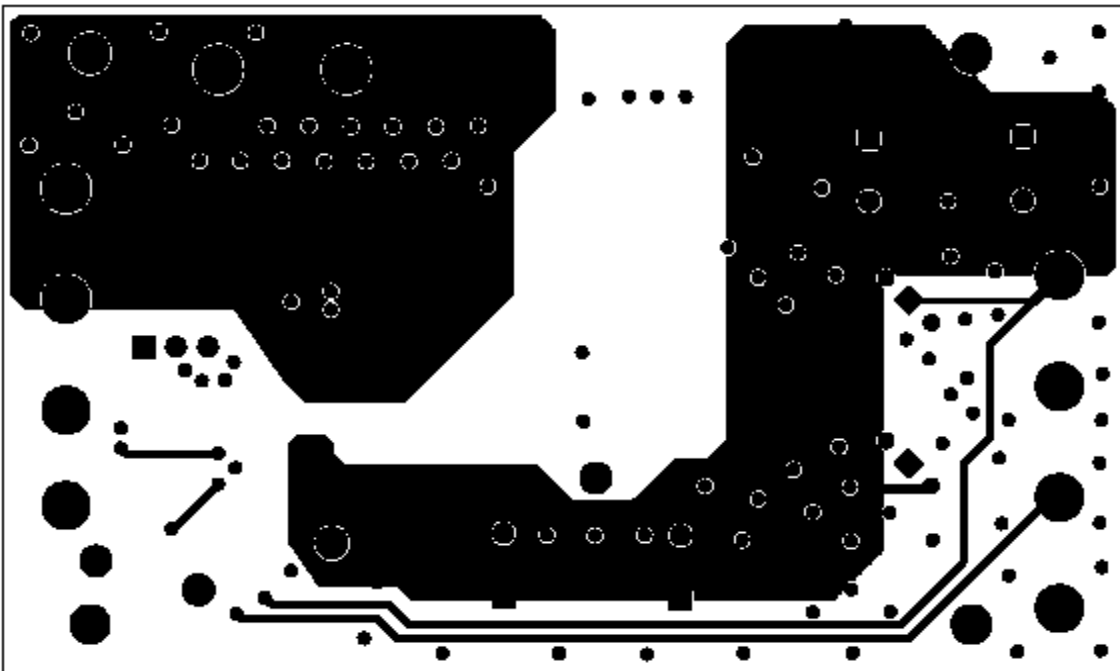


FIGURE 11. BOTTOM SILKSCREEN

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.

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